R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

SUPPORT FOR THE CLAIM AMENDMENTS

Support for the claim amendments may be found in the specification, for example, on page 13 lines 1-4, page 21 lines 3-5, and FIGS. 2, 3, 5 and 6, as originally filed. Thus, no new matter has been added. As the amendments remove the 35 U.S.C. §112, second paragraph rejection from issue for purposes of an appeal, the amendments should be entered per MPEP §714.13 II. If the amendments are not entered, Applicants respectfully request a concise explanation per MPEP §714.13 III in consideration of an appeal.

COMPLETENESS/FINALITY OF THE OFFICE ACTION

Aside from a notice of allowance, Applicant's representative respectfully requests any further action on the merits be presented as a **non-final** action. MPEP §706.07(a) states:

> Under present practice, second or any subsequent action on the merits shall be final, **except** where the examiner introduces a new ground of rejection that is neither necessitated by applicant's amendment of the claims nor based on information submitted in an information disclosure statement filed during the period set forth in 37 CFR 1.97(c) with the fee set forth in 37 CFR 1.17(p). (Emphasis added)

37 CFR §1.104(b) further states:

> (b) *Completeness of examiner's action.* The examiner's **action will be complete as to all matters**, except that in appropriate circumstances, such as misjoinder of invention, fundamental defects in the application, and the like, the action of the examiner may be limited to such matters of form need not be raised by the examiner until a claim is found allowable. (Emphasis added)

No arguments have ever been presented directed to dependent claims 12-17. The assertion in the current Office Action that "As per claims 11-17, refer to above-rejected claimed subject matter for claims 1-10 and the cited reference used for the rejection" does not provide any evidence or rational why claims 12-17 are allegedly anticipated. Note that there is **no similarly claimed subject matter** in claims 1-10 compared to claims 12-17. Therefore, the current Office Action is incomplete and the finality should be withdrawn. Since claims 12-17 have never received a proper first rejection, the next Office Action, if any, should be non-final per MPEP §706.07(a).

ANSWER ALL MATERIAL TRAVERSED

Applicant's representative respectfully requests that either a notice of allowance or a new office action on the merits be issued due to a lack of proper development for the rejection explanations. MPEP §707.07(f) states:

> In order to provide a complete application file history and to enhance the clarity of the prosecution history record, an

> examiner **must provide clear explanations** of all actions taken by the examiner during prosecution of an application.
> ...
> Where the applicant traverses any rejection, the examiner should, if he or she repeats the rejection, take note of the applicant's argument and **answer the substance** of it. (Emphasis added)

The current Office Action repeats the rejections for claims 12-17 but does not answer the substance of the traverse provided in the previous Amendment. As such, the current Office Action is incomplete and either a notice of allowance or a new Office Action should be issued.

CLAIM OBJECTION UNDER 35 U.S.C. §132

The objection to claim 20 under 35 U.S.C. §132 for new matter is respectfully traversed and should be withdrawn.

Claim 20 provides the assembly according to claim 10, further comprising **a fourth circuit** connected to a second circuit and configured process at least one of a plurality of first parameters in an incoming packet in accordance with a pointer. Claim 10 provides **a first circuit** configured to delineate a receive frame from a first network having a network protocol to produce the incoming packet; **a second circuit** configured to (i) store the pointer for each of the first parameters of the network protocol, (ii) process at least one of the first parameters in the incoming packet in accordance with the pointer to produce a second parameter, and (iii) present an outgoing packet containing the

second parameter; and **a third circuit** configured to frame the outgoing packet to present a transmit frame to a second network.

Referring to FIGS. 2 and 3 of the application, as originally filed, a Network 1 Interface circuit 122 may be representative of the claimed first circuit, a Protocol Processing Engine circuit 126 may be representative of the claimed second circuit, a Network 2 Interface circuit 124 may be representative of the claimed third circuit and an External Peripherals **circuit 108** may be representative of the **claimed fourth circuit**. Furthermore, the text of the application, as originally filed, states:

> The interface 114 may provide a mechanism to couple to the external circuit 108 to expand the parameter processing capability when desired. (Page 8, lines 18-20)
>
> The protocol processing engine 126 may be coupled to the interface 114 to exchange the parameters (e.g., signal PARAM) with the external circuit 108. The external circuit 108 may be operational to provide some parameter processing. (Page 11, lines 13-17)
>
> The external circuit 108 may be implemented a one or more circuits 132N-Q. (Page 13, lines 16-17)
>
> Each peripheral block 132A-Q may be designed to perform an operation on the parameters. (Page 14, lines 8-9)

Based on the above text, figures and claim 6, one of ordinary skill in the art would appear to understand that the Applicant had possession of the claimed fourth circuit at the time of filing. Therefore, claim 20 is fully compliant with 35 U.S.C. §132 and the objection should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §112

The rejection of claim 20 under 35 U.S.C. §112, first paragraph, written description is respectfully traversed and should be withdrawn.

The rejection of claims 10, 11 and 20 under 35 U.S.C. §112, second paragraph, indefiniteness, has been obviated by appropriate amendment and should be withdrawn.

Claim 20 provides a fourth circuit connected to a second circuit and configured process at least one of a plurality of first parameters in an incoming packet in accordance with a pointer. As noted above in the response to the 35 U.S.C. §132 rejection, claim 20 may be represented in the specification as the External Peripherals circuit 108. Furthermore, as illustrated in FIG. 3 of the application, the External Peripherals circuit 108 contains additional Peripheral circuits 132N-Q that are similar to the peripheral circuits 132A-132M within the Processing circuit 128 (part of the Protocol Processing Engine circuit 126). Therefore, one of ordinary skill in the art would appear to understand how to use and/or make the invention. As such, claim 20 is fully compliant with 35 U.S.C. §112, first paragraph, written description, and the rejection should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1-17 under 35 U.S.C. §102(e) as being anticipated by Dietz et al. '725 (hererafter Dietz) is respectfully traversed and should be withdrawn.

Dietz concerns a processing protocol specific information in packets specified by a protocol description language (Title).

37 C.F.R. §1.104(c)(2) states:

> In rejecting claims for want of novelty or for obviousness, the examiner must cite the best references at his or her command. When a reference is complex or shows or describes inventions other than that claimed by the applicant, the particular part relied upon must be designated as nearly as practicable. **The pertinence of each reference, if not apparent, must be clearly explained** and each rejected claim specified. (Emphasis added)

Claim 1 provides a database configured to store a pointer for each of a plurality of first parameters of a network protocol. While the Office Action never actually identifies the elements of Dietz allegedly similar to the claimed database and the claimed pointers, the cites into Dietz appear to suggest that either a CAM (column 21, lines 11-24) or a database of flows 324 (FIG. 15) of Dietz may be alleged similar to the claimed database. The cited text reads:

> The cache subsystem 1115 is an associative cache that includes a set of content addressable memory cells (CAMs) each including an address portion and **a pointer portion pointing to the cache memory** (e.g., RAM) containing the cached flow-entries. The CAMs are arranged as a stack ordered from a top CAM to a bottom CAM. The **bottom CAM's pointer** points to the least recently used (LRU) cache memory entry. Whenever there is a cache miss, the contents of cache memory pointed to by the bottom CAM are replaced by the flow-entry from the flow-entry database 324. This now becomes the most recently used entry, so the contents of the bottom CAM are moved to the top CAM and all CAM contents are shifted down. Thus, the cache is an associative cache with a true LRU replacement policy. (Column 21, liens 11-24)(Emphasis added)

The only "pointer" mentioned in the above text appears to be the CAM pointers pointing to a cache memory. However, Dietz appears to be silent that the "pointers" (asserted similar to the cache pointers) are for each of "a plurality of first parameters" (not identified in Dietz) of a network protocol. Therefore, the CAM and associated pointers of Dietz to not appear to be similar to the claimed database configured to store a pointer for each of a plurality of first parameters of a network protocol.

Furthermore, Dietz appears to be silent regarding the database of flows 324 in FIG. 15 (also possibly asserted similar to the claimed database) storing pointers for each of a plurality of first parameters of a network protocol. Therefore, the database of flows 324 of Dietz does not appear to be similar to the claimed database configured to store a pointer for each of a plurality of first parameters of a network protocol. As such, the Examiner is respectfully requested to either (i) clearly identify which elements of Dietz are allegedly similar to the claimed database and the claimed pointers and explain how the identified elements of Dietz allegedly anticipate the claim elements in accordance with 37 CFR §1.104(c)(2) or (ii) withdraw the rejection.

Claim 1 further provides a processing circuit configured to (i) process at least one of the first parameters in an incoming packet in accordance with the pointer to produce a second parameter. Assuming, *arguendo*, that either (i) the CAM pointers of

Dietz or (ii) the unidentified pointers allegedly stored in the database of flows 324 of Dietz are somehow similar to the claimed pointers (for which Applicant's representative does not necessarily agree), the cited text of Dietz appears to be silent regarding a processing circuit processing at least one of the first parameters in an incoming packet in accordance with the pointer to produce a second parameter. The cited text of Dietz reads:

> FIG. 15 shows how an embodiment of the network monitor 300 might be used to analyze traffic in a network 102. Packet acquisition device 1502 acquires all the packets from a connection point 121 on network 102 so that all packets passing point 121 in either direction are supplied to monitor 300. Monitor 300 comprises the parser sub-system 301, which determines flow signatures, and analyzer sub-system 303 that analyzes the flow signature of each packet. A memory 324 is used to store the database of flows that are determined and updated by monitor 300. **A host computer 1504, which might be any processor, for example, a general-purpose computer, is used to analyze the flows in memory 324.** As is conventional, host computer 1504 includes a memory, say RAM, shown as host memory 1506. In addition, the host might contain a disk. In one application, the system can operate as an RMON probe, in which case the host computer is coupled to a network interface card 1510 that is connected to the network 102. (Emphasis added)

While the Office Action never actually identifies an element of Dietz asserted similar to the claimed processing circuit, the cited text of Dietz suggests that a host computer 1504 may possibly be alleged similar to the claimed processing circuit. However, nowhere in the above text, or in any other section does Dietz appear to mention that the "processing circuit" (asserted similar to the host computer 1504 of Dietz) processes at least one of the "first parameters" (not identified in Dietz) in an incoming packet in accordance with the "pointer" (asserted similar to either the CAM pointers or some unidentified pointers allegedly stored in the database of flows 324 of Dietz). Furthermore, nowhere in the above

text, or in any other section does Dietz appear to mention that the "processing circuit" (asserted similar to the host computer 1504 of Dietz) produces the "second parameter" (not identified in Dietz) by processing the claimed "first parameter" (not identified in Dietz). Therefore, Dietz does not appear to disclose or suggest a processing circuit configured to (i) process at least one of the first parameters in an incoming packet in accordance with the pointer to produce a second parameter as presently claimed. As such, the Examiner is respectfully requested to either (i) clearly identify the elements of Dietz allegedly similar to the claimed processing circuit, the claimed first parameter and the claimed second parameter and explain how the alleged "processing circuit" element of Dietz produces the alleged "second parameter" element from the alleged "first parameter" element in accordance with 37 CFR §1.104(c)(2) or (ii) withdraw the rejection.

Claim 1 further provides the processing circuit configured to present an outgoing packet containing the second parameter. While the Office Action never actually identifies elements of Dietz asserted similar to the claimed processing circuit, the claimed second parameter and the claimed outgoing packet, the cites into Dietz suggest that a host computer 1504 of Dietz may be asserted similar to the claimed processing circuit and either (i) an Ethernet frame 1600 or (ii) an ATM cell of Dietz may

be asserted similar to the claimed outgoing packet. The cited text of Dietz reads:

> An offset field 1710 provides the offset to go to the next level information, i.e., to locate the start of the next layer level header. For the **Ethertype packet**, the start of the next layer header 14 bytes from the start of the frame.
> Other packet types are arranged differently. For example, in an ATM system, each ATM packet comprises a five-octet "header" segment followed by a forty-eight octet "payload" segment. The header segment of an **ATM cell** contains information relating to the routing of the data contained in the payload segment. The header segment also contains traffic control information. Eight or twelve bits of the header segment contain the Virtual Path Identifier (VPI), and sixteen bits of the header segment contain the Virtual Channel Identifier (VCI). Each ATM exchange translates the abstract routing information represented by the VPI and VCI bits into the addresses of physical or logical network links and routes each ATM cell appropriately. (Emphasis added)

Nowhere in the above text, or in any other section does Dietz appear to mention that the "outgoing packet" (asserted similar to either the Ethernet frame or ATM cell of Dietz) contains the "second parameter" (not identified in Dietz) produced by the "processing circuit" (asserted similar to the host computer 1504 of Dietz) from the "first parameter" (not identified in Dietz). Therefore, Dietz does not appear to disclose or suggest a processing circuit configured to present an outgoing packet containing a second parameter as presently claimed. As such, the Examiner is respectfully requested to either (i) clearly identify the elements of Dietz allegedly similar to the claimed processing circuit, the claimed first parameter and the claimed second parameter and explain how the identified elements of Dietz allegedly anticipate the claim limitations in accordance with 37 CFR §1.104(c)(2) or (ii) withdraw the rejection.

Claim 10 provides a second circuit configured to (i) store a pointer for each of a plurality of first parameters of a

network protocol. While the Office Action never actually identifies which elements of Dietz are allegedly similar to the claimed second circuit and the claimed pointers, the cites into Dietz appear to suggest that either a CAM (column 21, lines 11-24) or a database of flows 324 (column 15, lines 41-57 and FIG. 15) of Dietz are asserted similar to the claimed second circuit. The cited text of Dietz reads:

> The cache subsystem 1115 is an associative cache that includes a set of content addressable memory cells (CAMs) each including an address portion and **a pointer portion pointing to the cache memory** (e.g., RAM) containing the cached flow-entries. The CAMs are arranged as a stack ordered from a top CAM to a bottom CAM. The **bottom CAM's pointer** points to the least recently used (LRU) cache memory entry. Whenever there is a cache miss, the contents of cache memory pointed to by the bottom CAM are replaced by the flow-entry from the flow-entry database 324. This now becomes the most recently used entry, so the contents of the bottom CAM are moved to the top CAM and all CAM contents are shifted down. Thus, the cache is an associative cache with a true LRU replacement policy. (Column 21, lines 11-24)(Emphasis added)

> FIG. 15 shows how an embodiment of the network monitor 300 might be used to analyze traffic in a network 102. Packet acquisition device 1502 acquires all the packets from a connection point 121 on network 102 so that all packets passing point 121 in either direction are supplied to monitor 300. Monitor 300 comprises the parser sub-system 301, which determines flow signatures, and analyzer sub-system 303 that analyzes the flow signature of each packet. A memory 324 is used to store the database of flows that are determined and updated by monitor 300. A host computer 1504, which might be any processor, for example, a general-purpose computer, is used to analyze the flows in memory 324. As is conventional, host computer 1504 includes a memory, say RAM, shown as host memory 1506. In addition, the host might contain a disk. In one application, the system can operate as an RMON probe, in which case the host computer is coupled to a network interface card 1510 that is connected to the network 102. (Column 25, lines 41-58)

The only "pointer" mentioned in the above text appear to be the CAM pointers pointing to a cache memory. However, Dietz appears to be silent that the "pointer" (asserted similar to the cache memory pointers of Dietz) are for each of a plurality of the "first parameters" (not identified in Dietz) of a network protocol. Therefore, the CAM and associated pointers of Dietz to not appear to be similar to the claimed second circuit configured to store a

pointer for each of a plurality of first parameters of a network protocol.

Furthermore, Dietz appears to be silent regarding the database of flows 324 in FIG. 15 (also possibly asserted similar to the claimed second circuit) storing pointers for each of a plurality of first parameters of a network protocol. Therefore, the database of flows 324 of Dietz does not appear to be similar to the claimed second circuit configured to store a pointer for each of a plurality of first parameters of a network protocol. As such, the Examiner is respectfully requested to either (i) clearly identify the elements of Dietz allegedly similar to the claimed second circuit and the claimed pointers and explain how the identified elements of Dietz allegedly anticipate the claim limitations in accordance with 37 CFR §1.104(c)(2) or (ii) withdraw the rejection.

Claim 10 further provides the second circuit is configured to process at least one of the first parameters in the incoming packet in accordance with the pointer to produce a second parameter. While the Office Action never actually identifies elements of Dietz allegedly similar to the claimed second circuit, the claimed first parameter and the claimed second parameter, the cites into Dietz appear to suggest that either a CAM or a database of flows 324 of Dietz are being asserted similar to the claimed second circuit. The cited text of Dietz reads:

> The packet monitor 300 can analyze different protocols, and thus can perform different protocol specific operations on a packet wherein the protocol headers of any protocol are located at different locations depending on the parent protocol or protocols used in the packet. Thus, the packet monitor adapts to different protocols according to the contents of the packet. The locations and the information extracted from any packet are adaptively determined for the particular type of packet. For example, there is no fixed definition of what to look for or where to look in order to form the flow signature. In some prior art systems, such as that described in U.S. Pat. No. 5,101,402 to Chiu, et al., there are fixed locations specified for particular types of packets. With the proliferation of protocols, the specifying of all the possible places to look to determine the session becomes more and more difficult. Likewise, adding a new protocol or application is difficult. In the present invention, the number of levels is variable for any protocol and is whatever number is sufficient to uniquely identify as high up the level system as we wish to go, all the way to the application level (in the OSI model).
>
> Even the same protocol may have different variants. Ethernet packets for example, have several known variants, each having a basic format that remains substantially the same. An Ethernet packet (the root node) may be an Ethertype packet--also called an Ethernet Type/Version 2 and a DIX (DIGITAL-Intel-Xerox packet)--or an IEEE Ethernet (IEEE 803.x) packet. A monitor should be able to handle all types of Ethernet protocols. With the Ethertype protocol, the contents that indicate the child protocol is in one location, while with an IEEE type, the child protocol is specified in a different location. The child protocol is indicated by a child recognition pattern. (Column 32, line 50 - column 33, line 14)

Nowhere in the above text, or in any other section does Dietz appear to mention the "second circuit" (asserted similar to either the CAM or the database of flows 324 of Dietz) produce a "second parameter" (not identified in Dietz) by processing a "first parameter" (not identified in Dietz). Therefore, Dietz does not appear to disclose or suggest a second circuit configured to process at least one first parameter in an incoming packet in accordance with a pointer to produce a second parameter as presently claimed. As such, the Examiner is respectfully requested to either (i) clearly identify the elements of Dietz allegedly similar to the claimed second circuit, the claimed first parameter and the claimed second parameter and explain how the identified elements of Dietz allegedly anticipate the claim language in

accordance with 37 CFR §1.104(c)(2) or (ii) withdrawn the rejection.

Claim 10 further provides the second circuit is configured to present an outgoing packet containing the second parameter. While the Office Action never actually identifies which elements of Dietz that are allegedly similar to the claimed second circuit, the claimed outgoing packet and the claimed second parameter, the cites into Dietz suggest that either a CAM or a database of flows 324 of Dietz are being asserted similar to the claimed second circuit and either an Ethernet frame or ATM cell are being asserted similar to the claimed outgoing packet. The cited text of Dietz reads:

> The packet monitor 300 can analyze different protocols, and thus can perform different protocol specific operations on a packet wherein the protocol headers of any protocol are located at different locations depending on the parent protocol or protocols used in the packet. Thus, the packet monitor adapts to different protocols according to the contents of the packet. The locations and the information extracted from any packet are adaptively determined for the particular type of packet. For example, there is no fixed definition of what to look for or where to look in order to form the flow signature. In some prior art systems, such as that described in U.S. Pat. No. 5,101,402 to Chiu, et al., there are fixed locations specified for particular types of packets. With the proliferation of protocols, the specifying of all the possible places to look to determine the session becomes more and more difficult. Likewise, adding a new protocol or application is difficult. In the present invention, the number of levels is variable for any protocol and is whatever number is sufficient to uniquely identify as high up the level system as we wish to go, all the way to the application level (in the OSI model).
>
> Even the same protocol may have different variants. Ethernet packets for example, have several known variants, each having a basic format that remains substantially the same. An Ethernet packet (the root node) may be an Ethertype packet--also called an Ethernet Type/Version 2 and a DIX (DIGITAL-Intel-Xerox packet)--or an IEEE Ethernet (IEEE 803.x) packet. A monitor should be able to handle all types of Ethernet protocols. With the Ethertype protocol, the contents that indicate the child protocol is in one location, while with an IEEE type, the child protocol is specified in a different location. The child protocol is indicated by a child recognition pattern. (Column 32, line 50 - column 33, line 14)

> An offset field 1710 provides the offset to go to the next level information, i.e., to locate the start of the next layer level header. For the **Ethertype packet**, the start of the next layer header 14 bytes from the start of the frame.
>
> Other packet types are arranged differently. For example, in an ATM system, each ATM packet comprises a five-octet "header" segment followed by a forty-eight

> octet "payload" segment. The header segment of an **ATM cell** contains information relating to the routing of the data contained in the payload segment. The header segment also contains traffic control information. Eight or twelve bits of the header segment contain the Virtual Path Identifier (VPI), and sixteen bits of the header segment contain the Virtual Channel Identifier (VCI). Each ATM exchange translates the abstract routing information represented by the VPI and VCI bits into the addresses of physical or logical network links and routes each ATM cell appropriately. (Column 33, lines 51-67) (Emphasis added)

Nowhere in the above text, or in any other section, does Dietz appear to mention that a "second circuit" (asserted similar to either a CAM or a database of flows 324 of Dietz) presents "an outgoing packet" (asserted similar to either an Ethernet frame or an ATM cell of Dietz) containing a second parameter (not identified in Dietz). Therefore, Dietz does not appear to disclose or suggest a second circuit configured to present an outgoing packet containing a second parameter as presently claimed. As such, the Examiner is respectfully requested to either (i) clearly identify the elements of Dietz allegedly similar to the claimed second circuit, the claimed outgoing packet and the claimed second parameter and provide an explanation how the identified elements of Dietz allegedly anticipate the claim language in accordance with 37 CFR §1.104(c)(2) or (ii) withdraw the rejection.

Claim 10 further provides a third circuit configured to frame the outgoing packet to present a transmit frame to a second network. While the Office Action never actually identifies which elements of Dietz are allegedly similar to the claimed third circuit and the claimed transmit frame, the cites into Dietz (FIG. 15) suggest that a network interface card 1510 of Dietz is being

asserted similar to the claimed third circuit. The cited text of Dietz reads:

> The cache subsystem 1115 is an associative cache that includes a set of content addressable memory cells (CAMs) each including an address portion and a pointer portion pointing to the cache memory (e.g., RAM) containing the cached flow-entries. The CAMs are arranged as a stack ordered from a top CAM to a bottom CAM. The bottom CAM's pointer points to the least recently used (LRU) cache memory entry. Whenever there is a cache miss, the contents of cache memory pointed to by the bottom CAM are replaced by the flow-entry from the flow-entry database 324. This now becomes the most recently used entry, so the contents of the bottom CAM are moved to the top CAM and all CAM contents are shifted down. Thus, the cache is an associative cache with a true LRU replacement policy. (Column 21, lines 11-24)

> FIG. 15 shows how an embodiment of the network monitor 300 might be used to analyze traffic in a network 102. Packet acquisition device 1502 acquires all the packets from a connection point 121 on network 102 so that all packets passing point 121 in either direction are supplied to monitor 300. Monitor 300 comprises the parser sub-system 301, which determines flow signatures, and analyzer sub-system 303 that analyzes the flow signature of each packet. A memory 324 is used to store the database of flows that are determined and updated by monitor 300. A host computer 1504, which might be any processor, for example, a general-purpose computer, is used to analyze the flows in memory 324. As is conventional, host computer 1504 includes a memory, say RAM, shown as host memory 1506. In addition, the host might contain a disk. In one application, the system can operate as an RMON probe, in which case the host computer is coupled to a **network interface card 1510** that is connected to the network 102. (Column 25, lines 41-58) (Emphasis added)

Nowhere in the above text, or in any other section does Dietz appear to mention "a third circuit" (asserted similar to the network interface card 1510 of Dietz) is configured to frame "an outgoing packet" (asserted similar to either an Ethernet frame or an ATM cell in Dietz) to present "a transmit frame" (not identified in Dietz) to "a second network" (not identified in Dietz). Therefore, Dietz does not appear to disclose or suggest a third circuit configured to frame an outgoing packet to present a transmit frame to a second network as presently claimed. As such, the Examiner is respectfully requested to either (i) clearly identify the elements of Dietz which are allegedly similar to the claimed third circuit, the claimed outgoing packet, the claimed

transmit frame and the claimed second network and explain how the identified elements of Dietz allegedly anticipate the claim language in accordance with 37 CFR §1.104(c)(2) or (ii) withdrawn the rejection.

Claim 2 provides that the database is configured to store both an offset and a length for each first parameter. In rejecting claim 1, the Office Action appears to assert that either the CAM or the database of flows 324 of Dietz are similar to the claimed database. The Office Action further asserts that the above claim limitations are similar to the following text of Dietz:

> The PRE searches database 1001 and the packet in buffer 1008 in order to recognize the protocols the packet contains. In one implementation, the database 1001 includes a series of linked lookup tables. Each lookup table uses eight bits of addressing. The first lookup table is always at address zero. The Pattern Recognition Engine uses a base packet offset from a control register to start the comparison. It loads this value into a current offset pointer (COP). It then reads the byte at **base packet offset** from the parser input buffer and uses it as an address into the first lookup table.
>
> Each lookup table returns a word that links to another lookup table or it returns a terminal flag. If the lookup produces a recognition event the database also returns a command for the slicer. Finally it returns the value to add to the COP. (Column 19, lines 1-23)(Emphasis added)

The only "offset" mention above appears to be a "base packet offset". However, Dietz appears to be silent that the base packet offset is stored in the "database" (asserted similar to either the CAM or the database of flows 324 of Dietz). Furthermore, the base packet offset of Dietz does not appear to be for each "first parameter" (not identified in Dietz). Furthermore, no "lengths" appear to be mentioned in the above text. Furthermore, the above text of Dietz does not appear to mention that the "offsets" and "lengths" are stored in the "database" (asserted similar to either

the CAM or the database flows 324 of Dietz). Therefore, Dietz does not appear to disclose or suggest that the database is configured to store both an offset and a length for each first parameter as presently claimed. As such, the Examiner is respectfully requested to either (i) clearly identify the elements of Dietz allegedly similar to the claimed database, the claimed offset and the claimed length and explain how the identified elements allegedly anticipate the claim limitations or (ii) withdraw the rejection.

Claim 2 further provides that the processing circuit is further configured to partition each of the incoming packets in accordance with both of the offsets and the lengths to extract the first parameters. In rejecting claim 1, the Office Action appears to assert that a host computer 1504 of Dietz is allegedly similar to the claimed processing circuit. From the analysis above, the Office Action also appears to assert that a base packet offset of Dietz is allegedly similar to the claimed offset. The Office Action further asserts that the text in column 19, lines 16-61 is similar to the above claim limitations:

> The PRE 1006 includes of a comparison engine. The comparison engine has a first stage that checks the protocol type field to determine if it is an 802.3 packet and the field should be treated as a length. If it is not a length, the protocol is checked in a second stage. The first stage is the only protocol level that is not programmable. The second stage has two full sixteen bit content addressable memories (CAMs) defined for future protocol additions.
>
> Thus, whenever the PRE recognizes a pattern, it also generates a command for the extraction engine (also called a "slicer") 1007. The recognized patterns and the commands are sent to the extraction engine 1007 that extracts information from the packet to build the parser record. Thus, the operations of the extraction engine are those carried out in blocks 306 and 312 of FIG. 3. The commands are sent from PRE 1006 to slicer 1007 in the form of extraction instruction pointers which tell the extraction engine 1007 where to a find the instructions in the extraction operations database memory (i.e., slicer instruction database) 1002.

> Thus, when the PRE 1006 recognizes a protocol it outputs both the protocol identifier and a process code to the extractor. The protocol identifier is added to the flow signature and the process code is used to fetch the first instruction from the instruction database 1002. Instructions include an operation code and usually source and destination offsets as well as a length. The offsets and length are in bytes. A typical operation is the MOVE instruction. This instruction tells the slicer 1007 to copy n bytes of data unmodified from the input buffer 1008 to the output buffer 1010. The extractor contains a byte-wise barrel shifter so that the bytes moved can be packed into the flow signature. The extractor contains another instruction called HASH. This instruction tells the extractor to copy from the input buffer 1008 to the HASH generator.
>
> Thus these instructions are for extracting selected element(s) of the packet in the input buffer memory and transferring the data to a parser output buffer memory 1010. Some instructions also generate a hash.
>
> The extraction engine 1007 and the PRE operate as a pipeline. That is, extraction engine 1007 performs extraction operations on data in input buffer 1008 already processed by PRE 1006 while more (i.e., later arriving) packet information is being simultaneously parsed by PRE 1006. This provides high processing speed sufficient to accommodate the high arrival rate speed of packets.

Nowhere in the above text does Dietz appear to mention that the "processing circuit" (asserted similar to the claimed host computer 1504 of Dietz) is further configured to partition the incoming packet in accordance with the "offsets" (asserted similar to the claimed base packet offset of Dietz) and the "lengths" (not identified in Dietz) to extract the "first parameters" (not identified in Dietz). Therefore, Dietz does not appear to disclose or suggest a processing circuit configured to partition each of the incoming packets in accordance with both of the offsets and the lengths to extract first parameters as presently claimed. Claim 11 provides language similar to claim 2. As such, the Examiner is respectfully requested to either (i) clearly identify the elements of Dietz allegedly similar to the claimed processing circuit, the claimed offsets, the claimed lengths and the claimed first parameter and explain how the identified elements of Dietz

allegedly anticipate the claim limitations or (ii) withdrawn the rejection.

Claim 3 provides an interface directly connected to the database and configured to download all of the offsets, the lengths, and the pointers for storage in the database. In rejecting claims 1 and 2, the Office Action appears to assert that either the CAM or the database of flows 324 is similar to the claimed database, a base packet offset is similar to the claimed offsets and either CAM pointers or some unidentified pointers allegedly stored in the database of flows 324 of Dietz are allegedly similar to the claimed pointers. The Office Action further asserts that the above claim limitations are similar to the text in column 25, line 41-57 of Dietz:

> FIG. 15 shows how an embodiment of the network monitor 300 might be used to analyze traffic in a network 102. Packet acquisition device 1502 acquires all the packets from a connection point 121 on network 102 so that all packets passing point 121 in either direction are supplied to monitor 300. Monitor 300 comprises the parser sub-system 301, which determines flow signatures, and analyzer sub-system 303 that analyzes the flow signature of each packet. A memory 324 is used to store the database of flows that are determined and updated by monitor 300. A host computer 1504, which might be any processor, for example, a general-purpose computer, is used to analyze the flows in memory 324. As is conventional, host computer 1504 includes a memory, say RAM, shown as host memory 1506. In addition, the host might contain a disk. In one application, the system can operate as an RMON probe, in which case the host computer is coupled to a network interface card 1510 that is connected to the network 102. (Column 25, lines 41-58)

Nowhere in the above text, or in any other section does Dietz appear to mention an interface directly connected to the "database" (asserted similar to either the CAM or the database of flows 324 of Dietz) and configured to download all of the "offsets" (asserted similar to the base packet offset of Dietz), the lengths (not identified in Dietz), the pointers (asserted similar to either the

CAM pointers or some unidentified pointers in the database of flows 324 of Dietz) for storage in the "database" (asserted similar to either the CAM or the database of flows 324 of Dietz). Therefore, Dietz does not appear to disclose or suggest an interface directly connected to a database and configured to download all of the offsets, the lengths, and the pointers for storage in the database as presently claimed. As such, the Examiner is respectfully requested to either (i) clearly identify the elements of Dietz allegedly similar to the claimed interface, the claimed database, the claimed offsets, the claimed lengths and the claimed pointers and explain how the identified elements of Dietz allegedly anticipate the claim limitations or (ii) withdrawn the rejection.

Claim 4 provides a plurality of peripheral blocks each (ii) linked to the pointers and (iii) configured to perform a process involving the first parameters. In arguing claim 1, the Office Action appears to assert that either the CAM pointers or some unidentified pointers allegedly stored in the database of flows 324 of Dietz are similar to the claimed pointers. While the Office Action does not specifically identify the elements of Dietz allegedly similar to the claimed peripheral blocks, the Office Action does assert that the claimed peripheral blocks are similar to the text in column 25, lines 41-48 of Dietz:

> FIG. 15 shows how an embodiment of the network monitor 300 might be used to analyze traffic in a network 102. Packet acquisition device 1502 acquires all the packets from a connection point 121 on network 102 so that all packets passing point 121 in either direction are supplied to monitor 300. Monitor 300 comprises the parser sub-system 301, which determines flow signatures, and analyzer sub-system 303 that analyzes the flow signature of each packet. A memory 324 is

> used to store the database of flows that are determined and updated by monitor 300. A host computer 1504, which might be any processor, for example, a general-purpose computer, is used to analyze the flows in memory 324. As is conventional, host computer 1504 includes a memory, say RAM, shown as host memory 1506. In addition, the host might contain a disk. In one application, the system can operate as an RMON probe, in which case the host computer is coupled to a network interface card 1510 that is connected to the network 102. (Column 25, lines 41-58)

Nowhere in the above text, or in any other section does Dietz appear to mention a plurality of peripheral blocks each (ii) linked to the "pointers" (asserted similar to either the CAM pointers or some unidentified pointers allegedly stored in the database of flows 324 of Dietz) and (iii) configured to perform a process involving the "first parameters" (not identified in Dietz). Therefore, Dietz does not appear to disclose or suggest a plurality of peripheral blocks each (i) coupled to a parsing circuit, (ii) linked to the pointers and (iii) configured to perform a process involving the first parameters as presently claimed. As such, the Examiner is respectfully requested to either (i) clearly identify the elements of Dietz allegedly similar to the claimed peripheral blocks, the claimed pointers and the claimed first parameters and explain how the identified elements of Dietz allegedly anticipate the claim limitations or (ii) withdraw the rejection.

Claim 5 provides that the database is configured to store both a second offset and a second length for a second parameter of a second network protocol. In rejecting claim 1, the Office Action appears to assert that either the CAM or the database of flows 324 of Dietz are allegedly similar to the claimed database. While the Office Action does not clearly identify any elements of Dietz

allegedly similar to the claimed second offset, the claimed second length and the claimed second parameter, the Office Action does assert that elements similar to the claimed second offset, second length and second parameter are mentioned in column 19, lines 1-12 and column 19, lines 16-61 of Dietz:

> The PRE searches database 1001 and the packet in buffer 1008 in order to recognize the protocols the packet contains. In one implementation, the database 1001 includes a series of linked lookup tables. Each lookup table uses eight bits of addressing. The first lookup table is always at address zero. The Pattern Recognition Engine uses a base packet offset from a control register to start the comparison. It loads this value into a current offset pointer (COP). It then reads the byte at base packet offset from the parser input buffer and uses it as an address into the first lookup table.
>
> Each lookup table returns a word that links to another lookup table or it returns a terminal flag. If the lookup produces a recognition event the database also returns a command for the slicer. Finally it returns the value to add to the COP.
>
> The PRE 1006 includes of a comparison engine. The comparison engine has a first stage that checks the protocol type field to determine if it is an 802.3 packet and the field should be treated as a length. If it is not a length, the protocol is checked in a second stage. The first stage is the only protocol level that is not programmable. The second stage has two full sixteen bit content addressable memories (CAMs) defined for future protocol additions.
>
> Thus, whenever the PRE recognizes a pattern, it also generates a command for the extraction engine (also called a "slicer") 1007. The recognized patterns and the commands are sent to the extraction engine 1007 that extracts information from the packet to build the parser record. Thus, the operations of the extraction engine are those carried out in blocks 306 and 312 of FIG. 3. The commands are sent from PRE 1006 to slicer 1007 in the form of extraction instruction pointers which tell the extraction engine 1007 where to a find the instructions in the extraction operations database memory (i.e., slicer instruction database) 1002.
>
> Thus, when the PRE 1006 recognizes a protocol it outputs both the protocol identifier and a process code to the extractor. The protocol identifier is added to the flow signature and the process code is used to fetch the first instruction from the instruction database 1002. **Instructions include** an operation code and usually **source and destination offsets** as well as a **length**. The offsets and length are in bytes. A typical operation is the MOVE instruction. This instruction tells the slicer 1007 to copy n bytes of data unmodified from the input buffer 1008 to the output buffer 1010. The extractor contains a byte-wise barrel shifter so that the bytes moved can be packed into the flow signature. The extractor contains another instruction called HASH. This instruction tells the extractor to copy from the input buffer 1008 to the HASH generator.
>
> Thus these instructions are for extracting selected element(s) of the packet in the input buffer memory and transferring the data to a parser output buffer memory 1010. Some instructions also generate a hash.
>
> The extraction engine 1007 and the PRE operate as a pipeline. That is, extraction engine 1007 performs extraction operations on data in input buffer 1008 already processed by PRE 1006 while more (i.e., later arriving) packet information is being simultaneously parsed by PRE 1006. This provides high processing speed sufficient to accommodate the high arrival rate speed of packets. (Column 19, lines 1-61)(Emphasis added)

The Office Action appears to be asserting that (i) source and destination offsets of instructions from Dietz are similar to the claimed second offsets and (ii) a length of the instructions from Dietz are similar to the claimed second length. However, Dietz appear to be silent regarding the "database" (asserted similar to either the CAM or the database of flows 324 of Dietz) store both the "second offset" (asserted similar to the instruction source and designation offsets of Dietz) and the "second length" (asserted similar to the instruction lengths of Dietz) for the "second parameter" (not identified in Dietz) of a second network protocol (not identified in Dietz). Therefore, Dietz does not appear to disclose or suggest a database configured to store both a second offset and a second length for a second parameter of a second network protocol as presently claimed. As such, the Examiner is respectfully requested to either (i) clearly identify the elements of Dietz allegedly similar to the claimed database, the claimed second offsets, the claimed second lengths, the claimed second parameter and the claimed second network protocol and explain how the identified elements of Dietz allegedly anticipate the claim limitations or (ii) withdraw the rejection.

Claim 6 and 7 depend from claim 1 which is now believed to be allowable. Since the dependent claims contain all of the limitations of the independent claim, claims 6 and 7 are fully

patentable over the cited reference and the rejection should be withdrawn.

Regarding claims 12-17, the Office Action fails to provide any evidence or arguments that the claims 12-17 are anticipated by Dietz. Claims 12-17 do not provide language similar to the claims 1-10 as implied on page 12 of the Office Action. As such, *prima facie* anticipation has not established and the rejection of claims 12-17 should be withdrawn. Furthermore, the current Office Action is incomplete regarding claims 12-17 and a either a notice of allowance or a new non-final Office Action should be issued.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claim 18 under 35 U.S.C. §103(a) as being anticipated by Dietz in view of Ogawa et al. '966 (hereafter Ogawa) is respectfully traversed and should be withdrawn.

The rejection of claim 19 under 35 U.S.C. §103(a) as being anticipated by Dietz in view of Wilford et al. '247 (hereafter Wilford) is respectfully traversed and should be withdrawn.

The rejection of claim 20 under 35 U.S.C. §103(a) as being anticipated by Dietz in view of Yanagihara et al. '578 (hereafter Yanagihara) is respectfully traversed and should be withdrawn.

Dietz concerns a processing protocol specific information in packets specified by a protocol description language (Title). Ogawa concerns a data receiving device which enables simultaneous execution of processes of a plurality of protocol hierarchies and generates header end signals (Title). Wilford concerns an architecture for high speed class of service enabled linecard (Title). Yanagihara concerns a digital signal processor, processing method, digital signal recording/playback device and digital signal playback method (Title).

Claim 18 provides a plurality of framing circuits each configured to operate on a unique network protocol. In contrast, both Dietz and Ogawa appear to be silent regarding multiple framing circuits each configured to operate on a unique network protocol. Therefore, Dietz and Ogawa, alone or in combination, do not appear to teach or suggest a plurality of framing circuits each configured to operate on a unique network protocol as presently claimed.

Furthermore, the Office Action fails to provide clear and particular evidence of motivation to combine the references. In particular, the asserted motivation "because the framing circuits would enhance the handling the information associated with the packet, and the packet related information would help enhance the software to process information for the assembly" is not credited to any reference or knowledge generally available as required by MPEP §2142. Furthermore, the asserted motivation does not appear

to solve a problem per *In re Huston*. Therefore, the asserted motivation appears to be merely a conclusory statement. As such, claim 18 is fully patentable over the cited references and the rejection should be withdrawn.

Claim 19 provides a plurality of de-framing circuits each configured to operate on a unique network protocol. In contrast, both Dietz and Wilford appear to be silent regarding multiple de-framing circuits each configured to operate on a unique network protocol. Therefore, Dietz and Wilford, alone or in combination, do not appear to teach or suggest a plurality of de-framing circuits each configured to operate on a unique network protocol as presently claimed.

Furthermore, the Office Action fails to provide clear and particular evidence of motivation to combine the references. In particular, the asserted motivation "because the de-framing circuits would enhance the handling the information associated with the packet, and the packet related information would help enhance the software to process information for the assembly" is not credited to any reference or knowledge generally available as required by MPEP §2142. Furthermore, the asserted motivation does not appear to solve a problem per *In re Huston*. Therefore, the asserted motivation appears to be merely a conclusory statement. As such, claim 19 is fully patentable over the cited references and the rejection should be withdrawn.

Claim 20 provides a fourth circuit connected to the second circuit and configured process at least one of the first parameters in the incoming packet in accordance with the pointer. The Office Action fails to actually identify any elements of Yanagihara allegedly similar to the claimed second circuit, the claimed fourth circuit, the claimed first parameter and the claimed pointer. The Office Action merely states that the claimed fourth circuit is taught by Yanagihara in FIG. 10A and column 1, lines 51-66:

> This invention aims to make it possible to perform rapid decoding of video data and audio data in a receiver/demodulator if there is a program change when a DVCR of the aforesaid type continuously plays back a plurality of digital broadcast programs, and this data is then input to such a receiver/demodulator.
>
> This invention further aims to provide a digital signal recording/playback device and digital signal playback method wherein there is no break in video data and audio data when the output during speed change playback of such a DVCR is input to a receiver/demodulator and decoded.
>
> To resolve the above problems, the digital signal processor according to this invention is characterized in comprising **first means for selecting a transport stream corresponding to any channel from a transport stream** containing a plurality of multiplexed channels, **second means for separating video data** and audio data in any desired program ... (Column 1, lines 51-66)(Emphasis added)

The Office Action appears to be arguing that the first means and the second means of Yanagihara somehow teach or suggest the claimed second circuit and the claimed fourth circuit. However, nowhere in the above text, or in any other section does Yanagihara appear to mention that the a fourth circuit (asserted similar to either the first means or the second means of Yanagihara) is configured process at least one of the "first parameters" (not identified in Yanagihara) in the incoming packet in accordance with the "pointer" (not identified in Yanagihara). Therefore, Dietz and Yanagihara, alone or in combination, do not appear to teach or suggest a fourth

circuit connected to a second circuit and configured process at least one of the first parameters in an incoming packet in accordance with a pointer as presently claimed.

Furthermore, the Office Action fails to provide clear and particular evidence of motivation to combine the references. In particular, the asserted motivation "because the additional circuit would enhance the handling the information associated with the packet, and the packet related information would help enhance the software to process information for the assembly" is not credited to any or knowledge generally available reference as required by MPEP §2142. Furthermore, the asserted motivation does not appear to solve a problem per *In re Huston*. Therefore, the asserted motivation appears to be merely a conclusory statement. As such, claim 20 is fully patentable over the cited references and the rejection should be withdrawn.

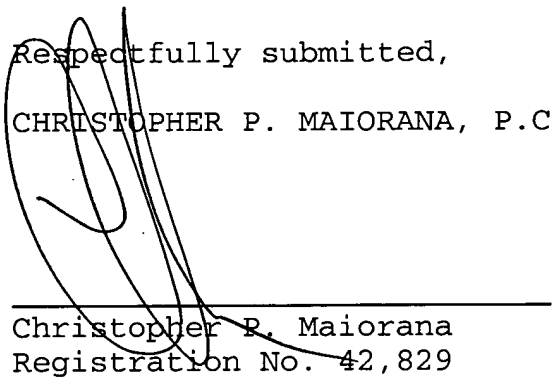
Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicant's representative should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge our office Account No. 50-0541.

Respectfully submitted,

CHRISTOPHER P. MAIORANA, P.C.



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